

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently Amended) An apparatus for routing data between
2 integrated circuit devices, comprising:
3 an n-dimensional grid of integrated circuit devices;
4 a plurality of communication networks coupling the n-dimensional grid of
5 integrated circuit devices, wherein a communication network of the plurality of
6 communication networks moves data unidirectionally in only orthogonal
7 dimensions; and
8 a routing mechanism configured to route data across the plurality of
9 communication networks as well as into, out of, and through a given integrated
10 circuit within the n-dimensional grid of integrated circuits;
11 whereby a process of routing signals across ~~a given network~~ a given
12 communication network is greatly simplified because it is not possible to create a
13 cycle that causes a deadlock within ~~the given network~~ the given communication
14 network; and
15 whereby the process of routing signals yields a shortest path between
16 source and destination.
- 1 2. (Original) The apparatus of claim 1, wherein the n-dimensional
2 grid of integrated circuit devices includes memory devices.

1 3. (Original) The apparatus of claim 1, wherein the n-dimensional
2 grid of integrated circuit devices includes processor devices, I/O devices, digital
3 signal processors, field programmable gate arrays, sensors, and controllers.

1 4. (Original) The apparatus of claim 1, wherein the plurality of
2 communication networks for a two-dimensional grid includes:
3 a first communication network configured to move signals East and North;
4 a second communication network configured to move signals North and
5 West;
6 a third communication network configured to move signals West and
7 South;
8 and
9 a fourth communication network configured to move signals South and
10 East.

1 5. (Original) The apparatus of claim 1, wherein the routing
2 mechanism is configured to statically route data items across the plurality of
3 communication networks.

1 6. (Original) The apparatus of claim 1, wherein the routing
2 mechanism is configured to dynamically route data items through network
3 junctions within each integrated circuit.

1 7. (Original) The apparatus of claim 1,
2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and

5 wherein during a dynamic routing process, the routing mechanism
6 removes a horizontal step or a vertical step from the header for the data item,
7 depending upon which direction is dynamically selected.

1 8. (Currently Amended) A method for creating a computing system,
2 comprising:
3 creating an n-dimensional grid of integrated circuit devices;
4 establishing a plurality of communication networks coupling the n-
5 dimensional grid of integrated circuit devices, wherein a communication network
6 of the plurality of communication networks moves data unidirectionally in only
7 orthogonal dimensions; and
8 providing a routing mechanism configured to route data across the
9 plurality of communication networks as well as into, out of, and through a given
10 integrated circuit within the n-dimensional grid of integrated circuits;
11 whereby a process of routing signals across ~~a given network~~ a given
12 communication network is greatly simplified because it is not possible to create a
13 cycle that causes a deadlock within ~~the given network~~ the given communication
14 network; and
15 whereby the process of routing signals yields a shortest path between
16 source and destination.

1 9. (Original) The method of claim 8, wherein the n-dimensional grid
2 of integrated circuit devices includes memory devices.

1 10. (Original) The method of claim 8, wherein the n-dimensional grid
2 of integrated circuit devices includes processor devices, I/O devices, digital signal
3 processors, field programmable gate arrays, sensors, and controllers.

1 11. (Original) The method of claim 8, wherein the plurality of
2 communication networks for a two-dimensional grid includes:
3 a first communication network configured to move signals East and North;
4 a second communication network configured to move signals North and
5 West;
6 a third communication network configured to move signals West and
7 South;
8 and
9 a fourth communication network configured to move signals South and
10 East.

1 12. (Original) The method of claim 8, wherein the routing mechanism
2 is configured to statically route data items across the plurality of communication
3 networks.

1 13. (Original) The method of claim 8, wherein the routing mechanism
2 is configured to dynamically route data items through network junctions within
3 each integrated circuit.

1 14. (Original) The method of claim 8,
2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and
5 wherein during a dynamic routing process, the routing mechanism
6 removes a horizontal step or a vertical step from the header for the data item,
7 depending upon which direction is dynamically selected.

1 15. (Currently Amended) A means for routing data between integrated
2 circuit devices within an n-dimensional grid of integrated circuit devices,
3 comprising:
4 a communication means comprising a plurality of communication
5 networks coupling the n-dimensional grid of integrated circuit devices, wherein a
6 communication network of the plurality of communication networks moves data
7 unidirectionally in only orthogonal dimensions; and
8 a routing means for routing data across the plurality of communication
9 networks as well as into, out of, and through a given integrated circuit within the
10 n-dimensional grid of integrated circuits;
11 whereby the means of routing signals yields a shortest path between source
12 and destination.

1 16. (Original) The means of claim 15, wherein the n-dimensional grid
2 of integrated circuit devices includes memory devices.

1 17. (Original) The means of claim 15, wherein the n-dimensional grid
2 of integrated circuit devices includes processor devices, I/O devices, digital signal
3 processors, field programmable gate arrays, sensors, and controllers.

1 18. (Original) The means of claim 15, wherein the plurality of
2 communication networks for a two-dimensional grid includes:
3 a first communication network configured to move signals East and North;
4 a second communication network configured to move signals North and
5 West;
6 a third communication network configured to move signals West and
7 South;
8 and

9 a fourth communication network configured to move signals South and
10 East.

1 19. (Original) The means of claim 15, wherein data is configured to
2 statically routed across the plurality of communication networks.

1 20. (Original) The means of claim 15, wherein data is dynamically
2 routed through network junctions within each integrated circuit.

1 21. (Original) The means of claim 15,
2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and
5 wherein during a dynamic routing process, a horizontal step or a vertical
6 step is removed from the header for the data item, depending upon which
7 direction is dynamically selected.